UNITED STATES PATENT APPLICATION

FOR

ENDPOINT DETECTION IN MANUFACTURING SEMICONDUCTOR DEVICE

BY

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DESCRIPTION OF THE INVENTION

Field of the Invention

[001] This invention relates in general to semiconductor device manufacturing and, more particularly, to a polish stop layer in a semiconductor layer for optical detection.

Background of the Invention

[002] In the semiconductor industry, it is generally required to form various material layers or structures over previously formed layers and structures in manufacturing semiconductor devices. However, the prior formations may leave the top surface topography of an in-process wafer highly irregular, for example, with bumps, trenches or other surface irregularities. These surface irregularities of the prior layers often cause problems to subsequent layers, resulting in poor yield and device performance. Accordingly, it is generally necessary to have a flat and planar surface through wafer planarization.

[003] A planarization method in the art for removing surface irregularities is chemical mechanical polishing ("CMP"). A CMP process may involve rotating a semiconductor wafer with respect to a polishing pad with slurry serving as a polishing agent between the wafer and the pad. A silicon oxide layer may be formed over the semiconductor wafer to protect a patterned layer previously formed on a surface of the wafer during the CMP process. The silicon oxide layer may include a thickness of approximately 10K to 20K angstroms (Å), which will then be polished to a thickness of approximately 5K to 10K Å.

[004] One problem with the CMP process is the proper determination of a planarization endpoint. In general, it is necessary to determine whether a wafer has been planarized to a desired flatness or thickness by detecting the surface characteristics of the wafer. Since it is not possible to perform the detection during a CMP process, one conventional method requires an operator to remove a control wafer from the CMP process, examine the control wafer for a desired endpoint, and load a production wafer into the CMP process. This conventional method of endpoint detection is labor-intensive and time-consuming.

[005] Another problem with the CMP process is the unequal elevation between a central portion and an edge portion of a polished wafer due to different rotation speeds between the central and edge portions of a polishing pad. The unequal elevation may lead to poor yield and device performance.

[006] Therefore, there is a general need in the art for a method to provide a more accurate determination of an endpoint in wafer planarization, and a more efficient way of detecting the endpoint for the CMP process.

SUMMARY OF THE INVENTION

[007] Accordingly, the present invention is directed to a method that obviates one or more of the problems due to limitations and disadvantages of the related art.

[008] To achieve these and other advantages, and in accordance with the purpose of the invention as embodied and broadly described, there is provided a method of manufacturing a semiconductor device that comprises the steps of providing a semiconductor wafer including a patterned layer, forming a first insulating layer over the patterned layer of the semiconductor wafer, the first

insulating layer including a first index of refraction, forming a second insulating layer over the first insulating layer, the second insulating layer including a second index of refraction smaller than the first index of refraction, removing the second insulating layer by a planarizing process, and detecting a change in index of refraction during the planarizing process.

[009] In one aspect, the method further comprises the step of ceasing the planarizing process when the change in index of refraction is detected.

[010] In another aspect, the method further comprises the step of removing a portion of the first insulating layer by the planarizing process when the change in index of refraction is detected.

[011] Also in accordance with the present invention, there is provided a method of endpoint detection for a chemical mechanical polishing (CMP) process in manufacturing a semiconductor device, the method comprising the steps of patterning a semiconductor wafer, forming a first insulating layer over the patterned semiconductor wafer, the first insulating layer including a first index of refraction, forming a second insulating layer over the first insulating layer, the second insulating layer including a second index of refraction smaller than the first index of refraction, removing the second insulating layer by the CMP process, detecting a change in index of refraction during the CMP process, and determining an endpoint for the CMP process.

[012] Still in accordance with the present invention, there is provided a method of endpoint detection for a chemical mechanical polishing (CMP) process in manufacturing a semiconductor device, the method comprising the steps of

providing a semiconductor wafer including a patterned layer, forming an insulating layer conformally with the patterned layer, the insulating layer including a first removal rate and a first index of refraction, forming a silicon oxide layer over the first insulating layer, the silicon oxide layer including a second removal rate greater than the first removal rate, and a second index of refraction smaller than the first index of refraction, removing the silicon oxide layer by the CMP process, detecting a change in index of refraction during the CMP process, and ceasing the CMP process when the change in index or refraction is detected.

[013] Further still in accordance with the present invention, there is provided a semiconductor device that comprises a semiconductor wafer having a patterned layer, a first insulating layer over the patterned layer, the first insulating layer having a first index of refraction, and a second insulating layer over the first insulating layer, the second insulating layer having a second index of refraction smaller than the first index of refraction, wherein the second insulating layer is removed by a planarization process when a change in index of refraction is detected.

[014] Additional objects and advantages of the invention will be set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

[015] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

[016] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate several embodiments of the invention and together with the description, serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[017] Figs. 1A to 1C are schematic diagrams illustrating the manufacturing of a semiconductor device in accordance with one embodiment of the present invention; and

[018] Fig. 2 is a graphical diagram illustrating a simulation result of a method in accordance with one embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[019] Reference will now be made in detail to the present embodiment of the invention, an example of which is illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[020] Figs. 1A to 1C are schematic diagrams illustrating the manufacturing of a semiconductor device 10 in accordance with one embodiment of the present invention. Referring to Fig. 1A, semiconductor device 10 includes a substrate 12 and a patterned layer 14. Substrate 12 may include various material layers or structures (not shown) depending on the desired functions of semiconductor device 10. Patterned layer 14 is formed over substrate 12, and generally includes a conductive layer comprised of polysilicon or metal such as aluminum or copper.

[021] Referring to Fig. 1B, prior to planarization by a planarizing process, a first insulating layer 16 is formed over patterned layer 14, and then a second

insulating layer 18 is formed over first insulating layer 16. In one embodiment according to the present invention, first insulating layer 16 is formed conformally with patterned layer 14 by chemical vapor deposition ("CVD"). As will be described in following paragraphs, first insulating layer 16 functions to serve as a polish stop layer for the CMP process. First insulating layer 16 includes a first removal rate and a first index of refraction. In one embodiment according to the present invention, the first removal rate is smaller than approximately 1000 Å per minute, and the first index of refraction is approximately 2. In another embodiment, first index of refraction is greater than 2. First insulating layer 16 may include silicon nitride (SiN), silicon oxide nitride (SiON) or silicon rich oxide ("SRO") of a thickness ranging from 500 to 2000 Å.

[022] Second insulating layer 18 has a second removal rate greater than the first removal rate of first insulating layer 16, and a second index of refraction smaller than the first index of refraction of first insulating layer 16. In one embodiment according to the present invention, the second removal rate is approximately three times the first removal rate, or 3000 Å per minute, and the second index of refraction is 1.4 and 1.5. Second insulating layer 18 may include silicon oxide of a thickness ranging from 10K to 20K Å.

[023] In another embodiment according to the invention, an oxide layer (not shown) is formed over patterned layer 14 before first insulating layer 16 is formed. The oxide layer functions to provide a planarized surface for first insulating layer 16.

[024] Referring to Fig. 1C, second insulating layer 18 is removed by performing a planarizing process, for example, a chemical mechanical polishing

("CMP") process to expose first insulating layer 16. In one embodiment according to the present invention, the CMP process is performed to expose a portion of first insulating layer 16, as shown with the dotted line in Fig. 1C. With a smaller removal rate than that of second insulating layer 18, it will be more difficult to polish away first insulating layer 16, which can be used as a polish stop for the CMP process. First insulating layer 16 can further alleviate the problem of unequal elevation between a central portion and edge portions of semiconductor device 10 after polishing. Moreover, with a greater index of refraction than that of second insulating layer 18, first insulating layer 16 can be used to determine an endpoint for the CMP process, as exemplarily described below with respect to Fig. 2.

[025] Fig. 2 is a diagram showing a simulation result of a method in accordance with one embodiment of the present invention. Referring to Fig. 2, curve A is an optical endpoint curve for a first semiconductor wafer being planarized by CMP for a first time period. Curve B is an optical endpoint curve for a second semiconductor wafer being planarized by CMP for a second time period shorter than the first time period. The first and second semiconductor wafers have the same material layers and structures, including a silicon nitride (SiN) layer and a silicon oxide (SiO_2) layer formed over the SiN layer. When a semiconductor wafer simply includes the SiN and SiO_2 layers without any underlying material layers or structures, the optical endpoint curve of that semiconductor wafer will behave like a sinusoidal wave.

[026] The simulation result shown in Fig. 2 is provided by a monitor (not shown) that includes a light source for radiating a laser beam toward a

semiconductor wafer under a CMP process, and a detector for detecting the strength of a laser beam reflected from the semiconductor wafer. The horizontal and vertical axes of Fig. 2 respectively represent the CMP processing time and the strength of a reflected laser beam. In one embodiment according to the present invention, the monitor is an in-situ removal monitor ("ISRM") mounted on a CMP polisher.

[027] Fig. 2 reveals a significant fall in the strength of the reflected laser beam in curves A and B. The fall results from a change in index of refraction, as will be described below. In general, the amplitude of the fall increases as the index of refraction increases, or as the CMP processing time increases. Since the first semiconductor wafer endures a longer CMP processing time than the second semiconductor wafer, the amplitude of the fall in curve A is greater than that in curve B. At the time point of approximately 120 seconds, the significant fall in the reflected light strength begins to occur because the SiO_2 layer is removed to an extent that exposes the SiN layer having a greater index of refraction than that of the SiO_2 layer. This time point, where a change in index of refraction occurs, can be used as an endpoint for the CMP process. To determine a CMP endpoint, a software program associated with the ISRM is generally employed to calculate the slope of curve A or B. The software program determines an endpoint for a CMP process where a continuous declining slope below a predetermined slope value is located.

[028] The present invention also provides a method of endpoint detection for a CMP process in manufacturing a semiconductor device. The method begins with providing a patterned semiconductor wafer. A first insulating layer having a first index of refraction is then formed over the patterned semiconductor wafer. A second

insulating layer is formed over the first insulating layer. The second insulating layer includes a second index of refraction smaller than the first index of refraction of the first insulating layer. The second insulating layer is removed by a CMP process. Next, a change in index of refraction during the CMP process is detected by a monitor. The monitor indicates an endpoint for the CMP process if the change in index of refraction is detected. The monitor subsequently sends a signal regarding the information of the endpoint to control software. The control software then ceases the operation of CMP devices in response to the signal sent from the monitor.

[029] The second insulating material formed at the edge portions is generally polished away quicker than the material formed at the central portions of a wafer. As a result, an endpoint can be determined prior to the total removal of the second insulating material formed at the central portions. In one embodiment according to the present invention, a portion, for example, 10% of thickness, of the first insulating layer is polished away by the CMP process to ensure complete planarization.

[030] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.